In the Specification

Page 1, Paragraph 3, kindly amend as follows:

With the advent of FPGA architectures having greater complexity, it is well understood by those of ordinary skill in the art that extensive digital systems can be implemented in FPGA devices. These FPGA devices may include many dockable elements such as D-Type flip flops and blocks of user assignable static random access memory (SRAM). The D-type flip flops and the user assignable SRAM in the FPGA device may either be synchronized to the same clock or to several different clocks. When a substantial number of these dockable elements are employed in a particular design, it is presently contemplated that at least one multi-level "clock tree" will be provided in the FPGA device.

Page 2, Paragraph 4, kindly amend as follows:

Multi-level clock trees are circuit devices that are well known to those of ordinary skill in the art. Typically, in a multi-level clock ~~free~~tree, a single lock source will drive the inputs to several clock buffers in the clock tree. This is known in the art as fanout. When the fanout becomes too large the clock signal will become unacceptably degraded. Accordingly, the fanout that a single source is permitted to drive is limited. The amount of fanout permitted depends upon the design being implemented. By implementing large clock buffers, limitations on the size of the fanout can be ameliorated. However, problems other than clock degradation also occur with the use of clock trees.

Page 4, Paragraph 9, kindly amend as follows:

It is another object of the present invention to provide a flexible interface between a DLL and the clock distribution trees, clock pads and signals from within an FPGA.

Page 4, Paragraph 12, kindly amend as follows:

According to the present invention, a delay locked loop (DLL) is employed in a field programmable gate array (FPGA) to align the active edge of a reference clock with a selected edge of a delayed clock, hereinafter referred to as the feedback clock. The reference clock may either be an internal or external clock signal, and the feedback clock is a clock signal that is derived from the reference clock signal, but has been delayed by some circuit in the FPGA, for example, a clock distribution tree. In the operation of the DLL, the feedback clock is farther delayed until ~~me~~the selected edge of the feedback clock is aligned with, but trailing by one cycle, the active edge of the reference clock. According to various aspects of the present invention, the feedback path of the feedback clock may be programmably selected to align the feedback clock to the reference clock at selected circuit nodes in the FPGA for the purpose of either deskewing the feedback clock or providing a 0 ns clock-to-out for the reference clock.

Page 6, Paragraph 22, kindly amend as follows:

In FIG. 1, a reference clock signal is supplied by either an INTERNAL CLOCK signal or EXTERNAL CLOCK signal that is programmably coupled by a programmable interconnect element 12 to the input 14 of a reference delay line 16, and the input 18 of a programmable delay line 20 in the DLL 10. When the EXTERNAL CLOCK is employed as the reference clock, the EXTERNAL CLOCK passes through an input buffer 22 having an associated delay. The sense of the reference clock may be inverted by an inverter 24 that is programmably disposed 1:1 in series with the input 14 to the reference

delay line 16. The output of the reference delay line 16 is coupled to a first input of a phase detector 26. The frequency of the reference may be halved by a divide-by-two circuit 28 that may be programmably disposed in series between the reference delay line 16 and the first input to the phase detector 26.

Page 7, Paragraph 23, kindly amend as follows:

In DLL 10, a feedback clock signal on conductor 30 is coupled to the input of a feedback delay line 32. The ~~sense~~phase of the feedback clock signal may be inverted by an inverter 34 that is programmably disposed in series with the input to the feedback delay line 32. The output of the feedback delay line 32 is coupled to a second input of phase detector 26. The frequency of the feedback ~~clod:~~clock signal passed through the feedback delay line 32 may be halved by a divide-by-two circuit 36 that is programmably disposed in series between the output of the feedback delay line 32 and the second input to the phase detector 26.

Page 11, Paragraph 31, kindly amend as follows:

According to the present invention, as described above, the DLL 10 can either be used to deskew a feedback clock so that it matches a reference clock or can be used to provide a 0 ns clock-to-out for the reference clock. When the DLL 10 is employed for clock deskew, the feedback clock path is picked off at the input to the flip-flop ~~42~~44, and when the DLL is employed for 0 ns clock-to-out the feedback clock path is picked off at the output of the input buffer 52. Various modes which implement these uses of the DLL 10 for the clock doubler ~~38~~40 and both the INTERNAL and EXTERNAL reference clocks will be described in greater detail below.

Page 11, Paragraph 32, kindly amend as follows:

In FIG. 2, a block diagram of the programmable delay line 20 is illustrated. The programmable delay line 20 includes a secondary delay line 60, a primary delay line ~~64~~62, and a pulse shaper 64. According to the present invention, the amount of delay provided by the secondary delay line 60 is controlled by four data bits from the control logic 38, and the amount of delay provided by the primary delay line 62 is controlled by eight data bits from the control logic 38. The data bits provided to the secondary delay line 60 by the control logic 38 are provided only during the acquisition mode of aligning the feedback clock signal to the reference clock signal, whereas, the primary delay line 62 is provided data by the control logic 38 during phase acquisition and then during maintenance to actively maintain phase lock during the normal operation of the FPGA after phase acquisition. The values controlling the secondary and primary delay lines 60 and 62, respectively, may be observed external to the FPGA on the SECST<0:3> and PRIST<0:7> status lines. The pulse shaper 64 is employed to compensate for any duty cycle distortion due to variations in the reference clock as a result of processing or temperature variations.

Page 12, Paragraph 33, kindly amend as follows:

It will be appreciated by those of ordinary skill in the art that there are many ways of implementing the primary and secondary delay lines 62 and 60, respectively, in a manner suitable for use according to the present invention. For example, the primary delay line may be implemented as eight groups, each having eight delay quanta. The eight control signals will then be provided to each of the eight groups. In this manner the primary delay line 62 may be tapped at two hundred and fifty-six locations by the eight control lines to provide the required delay in the primary delay line 62. The secondary delay line 60 can be implemented in a similar manner. Alternatively, the

primary and secondary delay lines 62 and 60 may be implemented using a delay quanta to form a binary weighted delay line or a segmented delay line in a manner well understood by those of ordinary skill in the art.

Page 13, Paragraph 35, kindly amend as follows:

In the delay quanta 70, the inverters 72 and 74 provide delay and the pass gate ~~80~~76 controls whether the delay quanta 70 is selected as the pick-off point in the programmable delay line 20. The primary delay line 62 provides fine tuning for the programmable delay line ~~22~~20, and the secondary delay line 60 provides coarse tuning for the delay line ~~22~~20. In a preferred embodiment, the parameters of the inverters 72 and 74 in the delay quanta 70 are chosen to provide approximately 100 ps of delay for each fine delay quanta in the primary delay line 62 and approximately 2.8 ns of delay for each coarse delay quanta in the secondary delay line 60.

Page 13, Paragraph 36, kindly amend as follows:

The reference delay line 16 and the feedback delay line 32 are included in the reference clock and feedback clock paths, respectively, to provide flexible timing control that permits the deskewed feedback clock edge to be moved forward or backward in time relative to the external clock. The reference delay line 16 and the feedback delay line 32 have adjustments according to preferred embodiment of approximately 690 ps that is programmable by four data bits. Like the programmable delay line 20, the reference delay 16 and the feedback delay line 32 may be implemented with delay quanta that are arranged in groups with taps or as binary weighted or segmented delay lines. The inclusion of the reference and feedback delay lines 16 and ~~30~~32 provides a convenient, responsive, and fine tunable trimming capability for difficult timing issues.

Page 15, Paragraph 40, kindly amend as follows:

In FIG. 4~~B~~C, the feedback clock is not delayed between points D and E. Rather, the reference clock is delayed between points A and B in an amount T6 by the reference delay line 16, and also by the programmable delay line 20 an amount which when added to the amount T4 results in a total delay in the amount of T7 produced by the programmable delay line 20. When the amount T7 is added to the delay T8 in the clock tree 42, the selected edge of the feedback clock effectively arrives later than the selected edge of the reference clock by the amount T6.

Page 15, Paragraph 41, kindly amend as follows:

Turning now to FIG. 5, a schematic diagram of a preferred embodiment of the clock doubler 40 according to the present invention is illustrated. In clock doubler 40, the reference clock (DBL IN) is fed into a quarter cycle delay line 100, a first input of an XOR gate 102, a first input of an AND gate 104, and through an inverter to a first input of an AND gate 106. The output of the quarter cycle delay line ~~110~~100 is coupled to a second input of the XOR gate 102, and the output of the XOR gate 102 is coupled to a second input of AND gates 104 and 106. The output of AND gate 104 is coupled to the input of a first duty cycle delay line 108, and the output of AND gate 106 is coupled to the input of a second duty cycle delay line 110. The outputs of first and second duty cycle delay lines 108 and 110 are coupled to first and second inputs of an OR gate 112. The output of OR gate 112 forms the output (DBL OUT) of the clock doubler 40.

Page 16, Paragraph 43, kindly amend as follows:

At trace J, it can be observed that the reference clock has been delayed one quarter cycle by the quarter cycle delay line 100 to determine the duty cycle of the clock at DBL OUT. The reference clock is then XORed with ~~me~~the output of the

quarter cycle delay line 100 by the XOR gate 102 to provide a doubled clock signal as depicted in trace X. As observed at trace X, if the duty cycle of the reference clock is not precisely 50%, there will be a difference in the resulting clock periods between alternate cycles following the XOR operation. To balance this jitter, the duty cycle delay lines 108 can be programmed to add further delays as depicted in traces A and B. In this manner, the traces B and D form the doubled clock output.

Page 19, Paragraph 50, kindly amend as follows:

In FIG. 7C, the mode illustrated is similar to that of the mode portrayed in FIG. 7B, except that the clocks are produced at the output pads ~~70~~50 that have zero delay relative to the external buffered clock, rather than zero clock-to-out.

Page 20, Paragraph 51, kindly amend as follows:

In FIG. 7E, the mode illustrated is similar to that shown in FIG. 7C, however, separate I/O pads 50-1 and 50-2 are employed instead of the single I/O pad 50, and the output and input buffers 46 and ~~52~~48 are separate buffers instead of a bidirectional buffer. In this implementation, a separate load ~~80~~70 can be connected to the I/O pads 50 so that input buffer ~~52~~48 is better matched to the input buffer 22 to provide a zero ns clock-to-out between the feedback clock and the reference clock. In this manner, the bondwire or package delays can be zeroed out by including them in the feedback loop, and the printed circuit board trace can be loaded between the two pads to match the slew rate on the input clock trace.

Page 20, Paragraph 52, kindly amend as follows:

FIG. 7F illustrates a mode that is similar to FIG. 7A, except that the clock doubler ~~38~~40 is included between the output of the programmable delay line 22 and the input to

the clock tree ~~40~~42 to double the frequency of the reference clock. In this mode, the delay in both the clock doubler and clock tree are zeroed out because they are included in the feedback loop.

Page 21, Paragraph 53, kindly amend as follows:

FIG. 7G illustrates a mode that is similar to FIG. 7B, except that the clock doubler ~~38~~40 is included between the output of the programmable delay line ~~22~~20 and the input to the clock tree ~~40~~42 to double the frequency of the reference clock. In this mode, it should be appreciated that the divide-by-two on the feedback input to the phase discriminator is not employed, because the divide-by-two-surrogate for the other array flip-flops carrying data cancels the clock doubler in the feedback path.